Q.P. Code: 20EC0402 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Regular Examinations May-2022

ELECTRONIC DEVICES AND CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Analyze the current components of a PN Junction Diode and derive the diode current equation.	L4	6M
	b	Show that the Zener diode can act as a voltage regulator with a circuit diagram.	L2	6M

OR

2	a	Derive the expression for transition capacitance of a PN junction diode.	L3	6M
	b	Construct the positive and negative diode clippers and explain with waveforms.	L3	6M

UNIT-II

3	a	Explain and derive the expressions for average DC current, RMS Value of current, DC Power output and AC Power input for a Full wave rectifier. List the advantages.	L3	6M
	b	Explain dynamic scattering LCD and field effect LCD with a diagram. List the advantages and applications.	L2	6M

OR

4	a	Demonstrate the working principle of LC filter with a circuit diagram and derive the expression for its ripple factor. List the advantages and disadvantages.	L4	6M
	b	Define tunneling phenomena and explain the V-I characteristics of a Tunnel diode with the help of energy band diagrams and List its applications.	L2	6M

UNIT-III

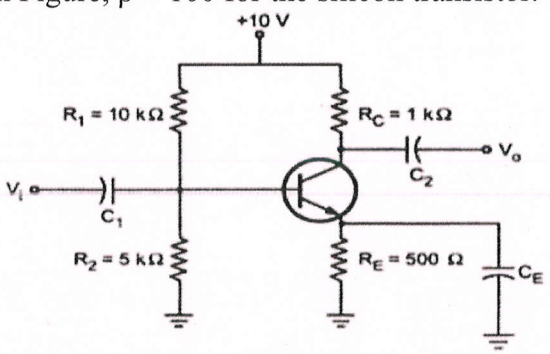
5	a	Define three regions of BJT operation. Explain the operation of an NPN transistor.	L2	6M
	b	Discuss about the construction and working principle of N-Channel JFET along with its characteristics.	L2	6M

OR

6	a	Define early effect. With a diagram, describe how a transistor acts as an amplifier.	L2	6M
	b	Differentiate the MOSFET with FET and explain the N-channel enhancement type MOSFET with characteristics.	L2	6M

UNIT-IV

7	a	Explain Collector to Base bias of a transistor with a circuit diagram and determine Q-point.	L2	6M
	b	For the circuit shown in Figure, $\beta = 100$ for the silicon transistor. Calculate V_{CE} and I_C.	L4	6M

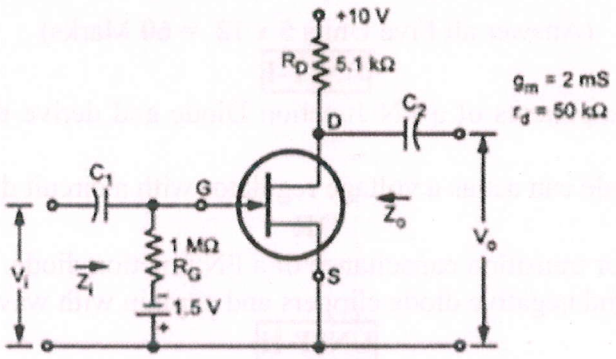


OR

8	a	Define and derive the stability factor 'S' for collector to base bias of BJT.	L3	6M
	b	Explain diode compensation technique for the parameters of V_{BE} and I_{CO}.	L2	6M

UNIT-V

9	a	Using low frequency h-parameter model, Evaluate the expressions for voltage gain, current gain, input impedance and output admittance for a BJT Amplifier in CE configuration.	L3	6M
	b	For the circuit shown in figure below, determine input impedance, output impedance and voltage gain.	L4	6M



OR

10	a	Examine the expressions for current gain, voltage gain, input impedance and output impedance of CB amplifier using simplified hybrid model.	L4	6M
	b	Summarize the expressions for input impedance, output impedance and voltage gain of JFET Common Drain amplifier with neat diagram.	L3	6M

*** END ***